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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/701,497	11/06/2003	Yoshitaka Sasago	XA-9693A	7623

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MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
SUITE 500
MCLEAN, VA 22102-3833

EXAMINER	
THOMAS, TONIAE M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 07/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/701,497	SASAGO ET AL.	
	Examiner	Art Unit	
	Toniae M. Thomas	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *29-47* is/are pending in the application.

4a) Of the above claim(s) *32-43* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *29 and 44-47* is/are rejected.

7)☒ Claim(s) *30 and 31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/166,145.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/06/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office action is responsive to the amendment filed on 19 April 2006. Currently, claims 29-47 are pending.

Information Disclosure Statement

2. The information disclosure statement filed on 06 November 2003 fails to comply with 37 CFR 1.98(a)(3) because it does not include a concise explanation of the relevance, as it is presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information, of each reference listed that is not in the English language. Therefore, the non-patent literature citation "The Japan Society of Applied Physics, Vol. 65, No. 11" has not been considered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 29 and 44-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. (US 6,232,173 B1) in view of Montree et al. (US 6,368,915 B1).

The Hsu et al. patent (Hsu) discloses a method for manufacturing a nonvolatile semiconductor memory device (figs. 5a-5l, 7a-7c, and

accompanying text). The method comprises: forming a well of a first conductivity in a semiconductor substrate (col. 8, lines 36-40); forming a pair of source and drain regions in the well, the source and drain regions being of a second conductivity type (figs. 7a and 5e)[1]; forming a first gate 209 on the substrate via a first gate insulator 206 (fig. 5b; col. 8, lines 47-52; col. 8, line 66 - col. 9, line 6 *and* fig. 5e and col. 9, lines 7-19); forming a second gate 218 on a second insulator 217 film covering the first gate (fig. 5h and col. 9, lines 41-45 *and* fig. 5i and col. 10, lines 10-20; forming a third gate, which is designated "control gate," via the second insulator film 217 relative to the first gate and via a third insulator film 211, 217 relative to the semiconductor substrate (figs. 5j, 5k and col. 10, line 51 - col. 11, line 5).

Hsu does not teach forming an impurity doped region of the first conductivity type, in this case p-type, in the channel region between the source and drain, wherein the impurity doped region is not in contact with the source and drain.

The Montree et al. patent (Montree) discloses a method for manufacturing a nonvolatile semiconductor memory device (figs. 1-12 and accompanying text). The method comprises: forming a silicon body 1 of a first

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[1] Figure 7a clearly shows that the source and drain regions, which are designated by "n+," are n-type semiconductor regions. This means that the stacked gate transistor in the nonvolatile memory area is an n-channel transistor. To render the transistor operable, the conductivity type of the well region in the nonvolatile memory area of the substrate must be opposite the conductivity type of the source drain regions. Thus, it is inherent that the conductivity of the well region in the nonvolatile memory portion of the substrate is p-type. Accordingly, for purposes of examination, the first conductivity type is p-type and the second conductivity type is n-type.

conductivity type, p-type (col. 10, lines 28-33); forming a source region 9, 11 and a drain region 9, 12 of a second conductivity type, n-type, in the silicon body (figs. 1, 2; col. 6, lines 35-42; and col. 6, lines 46-53); and forming an impurity doped region 16 of the first conductivity type in the channel region between the source and drain, wherein the impurity doped region is not in contact with the source and drain (fig. 6 and col. 7, lines 18-31).[2]

One of phosphorus and arsenic ions is used for the n-type impurity (col. 6, lines 35-42; and col. 6, lines 46-53), while boron ions are used for the p-type impurity (col. 7, lines 19-24).

Hsu and Montree are from the same field of endeavor, methods for manufacturing semiconductor devices and the devices formed therefrom. Thus, the purpose for which Montree is relied upon in this action would have been recognized in the primary prior art reference to Hsu by one of ordinary skill in the art at the time the invention was made.

It would have been obvious to one having ordinary skill in the, at the time the invention was made, to form an impurity doped region of the first conductivity type in the channel region between the source and drain regions, as taught by Montree, because the impurity doped region is capable of suppressing punchthrough between the source and drain regions (Montree - col. 7,lines 24-29).

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[2] In one embodiment, the impurity region 16 is used to suppress punchthrough between the source and drain (). In order for the region 16 to function in this capacity, it must have a higher dopant concentration than the silicon body 1.

Neither Hsu nor Montree explicitly disclose an embodiment, wherein the first conductivity type is n-type and the second conductivity type is p-type. However, in the fabrication of devices comprising MOS transistors, it is routine and well known in the art to form devices such that the first conductivity type is n-type and the second conductivity type is p-type. The selection is made according to the type of transistor the device requires, an n-channel MOS transistor or a p-channel MOS transistor. It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to form the nonvolatile memory device of Hsu such that the first conductivity type is n-type and the second conductivity type is p-type, because the method of Hsu and Montree is applicable to both n-channel devices and p-channel devices.

Allowable Subject Matter

4. Claims 30 and 31 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments filed 19 April 2006 have been fully considered but they are not persuasive. Applicant argues that neither the Hsu et al. or Montree et al. patents teach or suggest forming a third gate via the second insulator film relative to the first gate and via a third insulator film relative to the semiconductor substrate. As discussed above, Hsu et al. discloses forming a third gate via the second insulator film 217 relative to the first gate and via a

third insulator film 211, 217 relative to the semiconductor substrate. Therefore, the amendment filed on 19 April 2006 has not overcome the rejection of claim 29 under 35 USC 103(a) as being unpatentable over the combination of Hsu et al. and Montree et al.

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday through Friday from 8:30 a.m. to 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TMT
10 July 2006

Mary Wilczewski
Primary Examiner